Section 103 Rejections:

Claims 1-5, 7-8, 10-22, and 24-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,337,285 to Ko (hereinafter "Ko '285") in view of U.S. Patent No. 5,314,575 to Yanagida (hereinafter "Yanagida"). Claims 9 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ko '285 and Yanagida in view of U.S. Patent No. 6,117,791 to Ko (hereinafter "Ko '791"). In addition, claims 1-5 and 7-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,025,255 to Chen et al. (hereinafter "Chen") in view of Yanagida. Claim 19 has been canceled rendering rejection thereto moot. As set forth in more detail below, rejections of claims 1-5, 7-18, and 20-27 are respectfully traversed.

To establish *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); and, MPEP 2143.01. None of the cited art teaches or suggests all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

None of the cited art teaches or suggests an etch chemistry in which the etch chemistry is substantially free of hydrogen and selective to silicon nitride. Independent claim 1 recites in part:

> . . . etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen . . . and etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry, wherein the first and second etch chemistries are selective to silicon nitride.

As set forth in more detail below, Ko '285, Yanagida, Chen, and Ko '791 do not teach or suggest all limitations of claim 1.

Ko '285 discloses a two-step dual-chemistry process for etching through a selected portion of an insulating oxide layer. (Ko '285, Abstract). Ko '285 does not teach or suggest an etch chemistry where the etch chemistry is substantially free of hydrogen and selective to silicon nitride. In fact, the Office Action admits that Ko '285 "does not expressly teach that said first etch chemistry must be substantially free of hydrogen." (Office Action, page 3). Consequently, Ko '285 does not teach or suggest all limitations of present claim 1.

In addition, Yanagida cannot be combined with Ko '285 to overcome the deficiencies therein. Yanagida teaches away from an etch chemistry where the etch chemistry is substantially free of hydrogen and selective to silicon nitride. In particular, Yanagida discloses "[t]he silicon compound film to be etched in the method of the invention is a film made of various silicon compounds such as oxides, nitrides and the like of silicon and is not critical provided that it can be etched. SiO_2, silicon nitrides such as Si_3N_4, and the like will be effectively etched." (Yanagida, column 3, lines 33-38. Emphasis added). However, Ko '285 discloses a method that achieves etching of a doped oxide region while selective to silicon nitride. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). MPEP 2145 (X)(D)(2).

To combine the invention of Yanagida and Ko '285, as suggested in the Office Action, would be contrary to the intentions of Ko'285. For example, Yanagida discloses "a silicon compound film such as SiO_2 film or SiN film is dry etched in a pattern by a two-stage procedure wherein high speed anisotropic etching is first effected using a gas mainly composed of a H-free carbon fluoride gas such as C_3F_8, C_2F_6." (Yanagida, column 6, lines 34-38. Emphasis added). However, Ko '285 discloses that the first and second etching steps must include "good selectivity to the silicon nitride cap and silicon nitride spacers on the gate stack structures" and are intended to etch a doped oxide dielectric layer "without substantially damaging the nitride layer or the gate stack." (Ko '285, column 3, lines 25-41). As such, Yanagida cannot be combined with Ko '285 because such a combination would result in the etching of the silicon nitride layers of the gate stack causing damage to the underlying field oxide isolation regions. Consequently, Yanagida cannot be combined with Ko '285 to teach or suggest all limitations of claim 1.

Chen discloses a two-step etching process for forming self-aligned contacts. (Chen, Title). Chen does not teach or suggest an etch chemistry where the etch chemistry is substantially free of hydrogen and selective to silicon nitride. Chen discloses that the first etching step includes "an etchant gas mixture containing fluorocyclobutante (C_4F_8) . . . and CH_3F." (Chen, column 5, lines 49-51, emphasis added). In fact, the Office Action admits "Chen et al fails to teach that said first etch chemistry is substantially free of hydrogen." (Office Action, page 6). As such, Chen does not teach or suggest all limitations of claim 1.

In addition, Yanagida cannot be combined with Chen to overcome the deficiencies therein. As described above, Yanagida teaches a method that is not selective to silicon nitride and hence, may effectively etch such material with the etchant. However, Chen discloses a method to "[protect] the nitride cap 24 and exposed regions of the [silicon nitride] sidewalls 27." (Chen, column 6, lines 6-7). It

is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). MPEP 2145 (X)(D)(2). The statement in the Office Action suggesting "to combine the teaching of Yanagida to the process of Chen et al," is hereby respectfully traversed. (Office Action, page 6).

Chen discloses that the first etching step comprising both C_4F_8 and CH_3F "results in a relatively thick steady state polymer buildup over the silicon nitride top caps 24 and sidewalls 27 when the etch front reaches them." (Chen, column 5, lines 59-61). The polymer buildup is used to protect the silicon nitride sidewalls and silicon nitride cap, as shown in Fig. 4E and Fig. 4F. Once the etching process step is done, the polymer buildup is subsequently removed, resulting in no erosions of the nitride layers. To combine Yanagida and Chen, as suggested by the Office Action would not allow the polymer buildup to form and results in the etching of the nitride layers. Therefore, Yanagida cannot be combined with Chen to teach or suggest all limitations of claim 1.

Ko '791 discloses etching doped silicon dioxide. (Ko '791, Abstract). However, Ko '791 does not teach or suggest an etch chemistry where the etch chemistry is substantially free of hydrogen and selective to silicon nitride. In fact, Ko '791 discloses a one step etch chemistry, in which "[t]he doped silicon dioxide etchant of the present invention, $\underline{C_2H_xF_y}$ is a primary etchant." (Ko '791, column 5, lines 3-4, emphasis added). As such, Ko '791 does not disclose an etchant substantially free of hydrogen atoms. Therefore, Ko '791 does not teach or suggest all limitations of claim 1.

None of the cited art teaches or suggests a dielectric layer comprising doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. % or a dielectric layer comprising doped silicon oxide having a boron concentration of less than approximately 5 wt. %, as recited in independent claims 17 and 21, respectively. Amended independent claim 17 recites in part: "[a] method for forming a contact hole, comprising: depositing a dielectric layer upon first and second gate . . . wherein the dielectric layer comprises doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %." Amended independent claim 21 recites in part: "[a] method for forming a self aligned contact hole, comprising: etching a first portion of a substantially continuous dielectric layer . . . wherein the dielectric layer comprises doped silicon oxide having a boron concentration of less than approximately 5 wt. %." Support for the amendments to independent claims 17 and 21 may be found, for example, on page 12, lines 16-21 of the Specification.

Ko '285, Ko '791, and Chen disclose a deposition of a layer of phosphorus silicate glass (PSG) or borophosphorus silicate glass (BPSG). However, Ko '285, Ko '791, and Chen do not teach the layer comprising doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. % or doped silicon oxide having a boron concentration of less than approximately 5 wt. %. Furthermore, Yanagida does not disclose a layer of PSG or BPSG or a layer comprising of phosphorus concentration or boron concentration. As such, Ko '285, Ko '791, Chen, and Yanagida do not teach or suggest all limitations of claims 17 and 21.

Additionally, there is no motivation within Ko '285, Ko '791, Chen, and Yanagida to teach or suggest all limitations of claims 17 and 21. As indicated on page 4, line 28 through page 5, line 4 of the Specification, lightly or heavily doped dielectric materials may be used to obtain desired etch rates with conventional etch chemistries. For example, a lightly doped dielectric layer may have a "slow etch rate" whereas a heavily doped dielectric layer may have a "fast etch rate," with respect to each other. A lightly doped dielectric layer (e.g., phosphorus concentration of less than approximately 6 wt. % or boron concentration of less than approximately 5 wt. %), as recited in claims 17 and 21, may however, "not be selective to isolation regions which may be formed in an underlying semiconductor layer" using conventional etch chemistry. (Specification, page 6, lines 5-6). As such, an appropriate etch stop layer may be used to prevent the etching of the isolation region. The presently claimed case, however, presents an etch chemistry which may be selective to isolation regions while etching a lightly doped dielectric without the use of an underlying etch stop layer. Consequently, the limitation of claims 17 and 21 to include a lightly doped dielectric is distinct over the cited art.

In addition to not specifically teach the use of a lightly doped dielectric layer, Ko '285, Ko '791, Chen, and Yanagida do not teach using an etch stop layer for protecting an isolation region formed in an underlying semiconductor layer. As such, there is no motivation for Ko '285, Ko '791, Chen, and Yanagida to include a doped dielectric layer having a phosphorus concentration of less than approximately 6 wt. % or a boron concentration of less than approximately 5 wt. %. In addition, since an etch stop layer is not disclosed, one skilled in the art may presume a highly doped dielectric material (e.g., a phosphorus concentration of more than approximately 6 wt. % or a boron concentration of more than approximately 5 wt. %) is used in the invention of Ko '385, Ko '791, Chen, and Yanagida. Consequently, Ko '385, Ko '791, Chen, and Yanagida do not teach, suggest, or provide motivation for all limitations of claims 17 and 21.

For at least the reasons stated above, none of the cited art, either individually or in combination, teaches or suggests the limitations of claims 1, 17, and 21. Therefore, claims 1, 17, and 21, and claims dependent therefrom, are patentably distinct over the cited art. Accordingly, removal of the § 103(a) rejections of claims 1-5 and 7-27 are respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the final Office Action mailed November 19, 2002. In view of the remarks traversing the rejections, Applicant asserts that pending claims 1-5, 7-18, and 20-27 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 03-2769/5298-04100.

Respectfully submitted,

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ATTACHMENT A
"Marked-Up" Amendments

IN THE CLAIMS

Please cancel claim 19. Please amend claims 17 and 21 as follows. Also following is a list of all claims in their pending form.

1. (Twice Amended) A method for forming a semiconductor device, comprising:

etching a first portion of a dielectric layer formed on a semiconductor topography with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen and comprises C_4F_8; and

etching a second portion of the dielectric layer with a second etch chemistry different from the first etch chemistry, wherein the first and second etch chemistries are selective to silicon nitride.

2. The method of claim 1, wherein the dielectric layer is substantially continuous.

3. The method of claim 1, wherein an interface does not exist between the first and second portions of the dielectric layer.

4. The method of claim 1, wherein a thickness of the first portion of the dielectric layer is greater than a thickness of the second portion of the dielectric layer.

5. (Twice Amended) The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, and wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the gate structure.

6. (Canceled)

7. The method of claim 1, wherein the first etch chemistry further comprises CO.

8. The method of claim 1, wherein the second etch chemistry comprises at least one hydrogen-containing compound.

9. The method of claim 1, wherein the second etch chemistry comprises $C_2H_2F_4$.

10. The method of claim 1, wherein the second etch chemistry comprises CHF_3.

11. The method of claim 1, further comprising forming said dielectric layer on said semiconductor topography in one processing step.

12. The method of claim 1, wherein the first etch chemistry has a dielectric material: silicon nitride selectivity of at least approximately 10:1, and wherein the dielectric layer comprises the dielectric material.

13. The method of claim 1, wherein the second etch chemistry has a dielectric material: silicon oxide selectivity of at least approximately 5:1, and wherein the dielectric layer comprises the dielectric material.

14. The method of claim 1, wherein the dielectric layer comprises a doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %.

15. The method of claim 1, wherein the semiconductor topography comprises a gate structure formed on a semiconductor layer, wherein the semiconductor layer comprises isolation regions, and wherein the dielectric layer is in contact with a sidewall spacer of the gate structure and the semiconductor layer.

16. The method of claim 15, wherein etching the first portion of the dielectric layer exposes an upper corner of the sidewall spacer, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

17. (Twice Amended) A method for forming a contact hole, comprising:

depositing a dielectric layer upon first and second [gate] laterally spaced gate structures on a semiconductor layer comprising isolation regions, wherein the dielectric layer comprises doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %;

etching a first portion of the dielectric layer with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen; and

etching a second portion of the dielectric layer with a second etch chemistry, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the first and second gate structures.

18. The method of claim 17, wherein the first etch chemistry is selective to silicon nitride, and wherein the second etch chemistry is selective to silicon dioxide.

19. (Canceled)

20. The method of claim 17, wherein etching the first portion of the dielectric layer exposes upper corners of the first and second gate structures, and wherein etching the second portion of the dielectric layer exposes the semiconductor layer.

21. A method for forming a self aligned contact hole, comprising:

etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall spacer of said gate structure, wherein the dielectric layer comprises doped silicon oxide having a boron concentration of less than approximately 5 wt. %; and

etching a second portion of the substantially continuous dielectric layer with a second etch chemistry comprising a hydrofluorocarbon etchant sufficiently to expose a substrate under said substantially continuous dielectric layer.

22. The method of claim 17, wherein the dielectric layer is substantially continuous.

23. The method of claim 17, wherein the second etch chemistry comprises $C_2H_2F_4$.

24. The method of claim 17, wherein the dielectric layer is in contact with a sidewall spacer of the first and second gate structures and the semiconductor layer.

25. The method of claim 17, wherein the first etch chemistry has a dielectric material: silicon nitride selectivity of at least approximately 10:1, and wherein the dielectric layer comprises the dielectric material.

26. The method of claim 17, wherein the second etch chemistry has a dielectric material:silicon oxide selectivity of at least approximately 5:1, and wherein the dielectric layer comprises the dielectric material.

27. The method of claim 21, wherein the substrate under said substantially continuous dielectric layer comprises isolation regions, and wherein the isolation regions comprise undoped SiO_2.